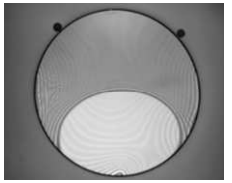
DIRECT WAFER BONDING AT LETI

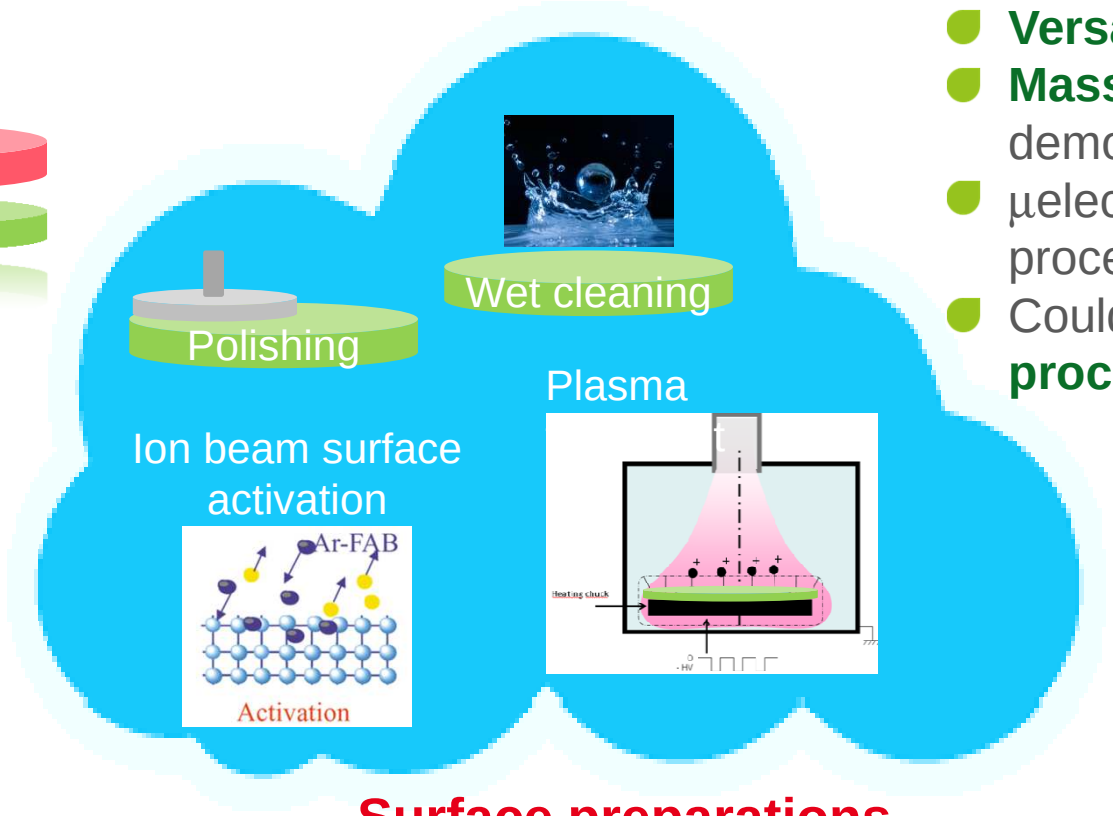
Leti Innovation Days | June 28-29, 2017

Frank Fournel
Head of wafer bonding engineering

DIRECT WAFER BONDING



"spontaneous bonding at room temperature without polymer"



- **Versatile** process
- **Mass production** demonstrated
- µelectronics and µtechnology processes **compatibility**
- Could be a **low temperature process**

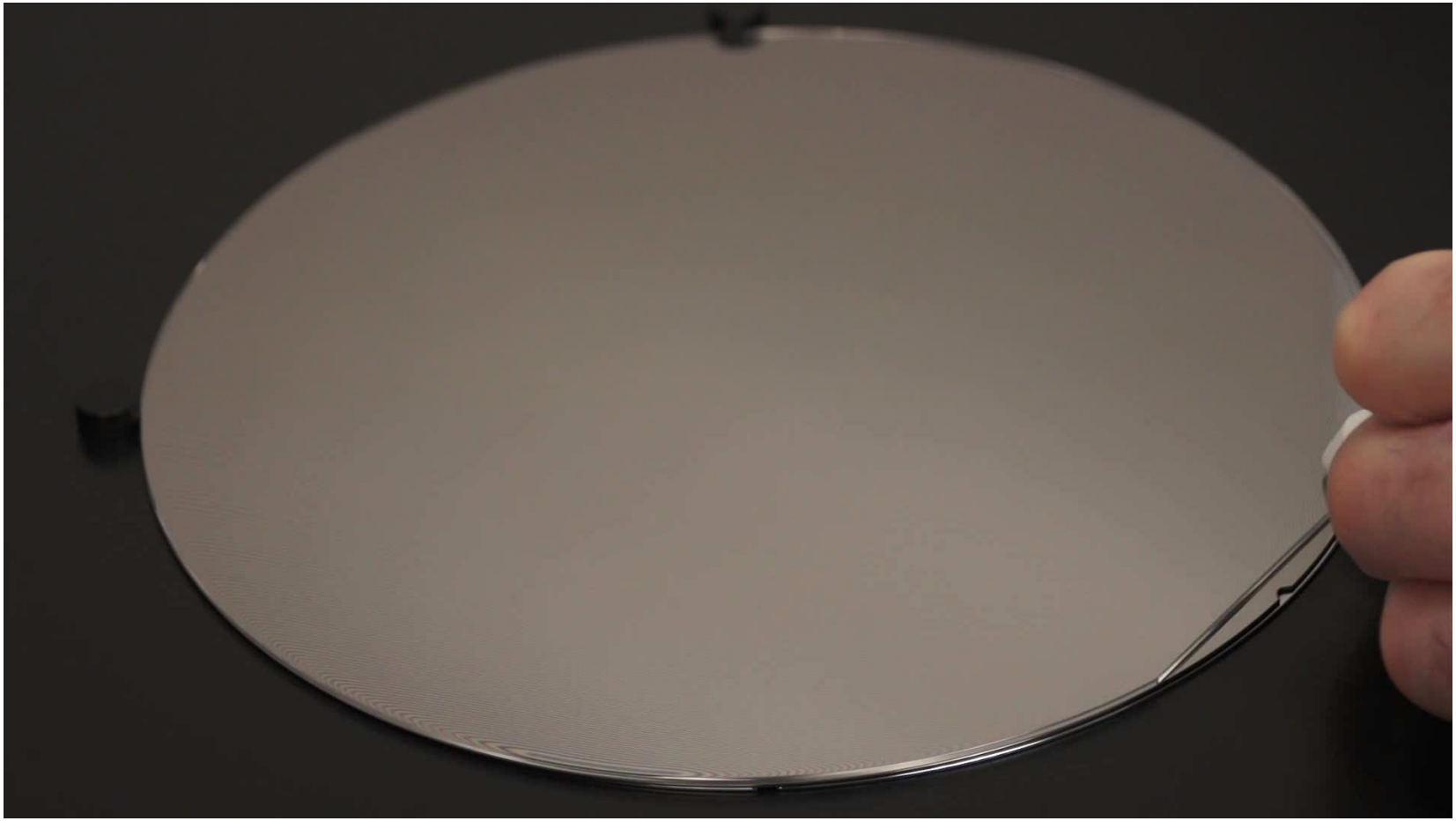
Surface preparations

Bonding

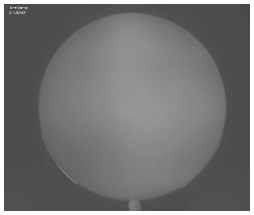
- **Critical surface preparations** (roughness, flatness, defect level…)

DIRECT WAFER BONDING

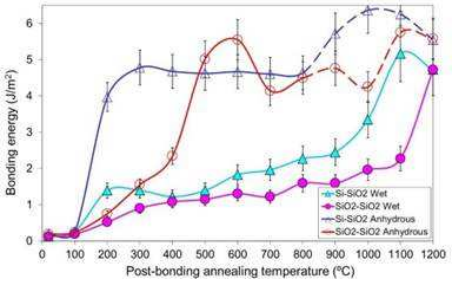
"spontaneous bonding at room temperature without polymer"

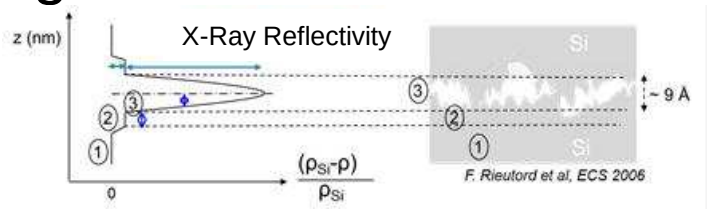


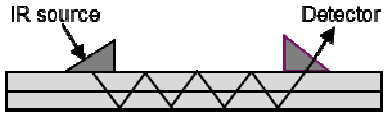
SILICON DIRECT WAFER BONDING

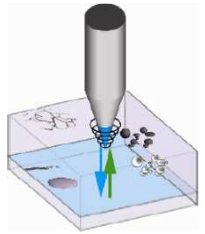


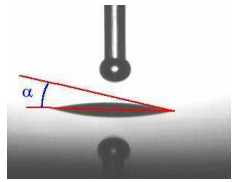
Direct bonding studies

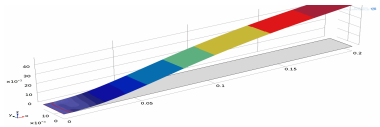




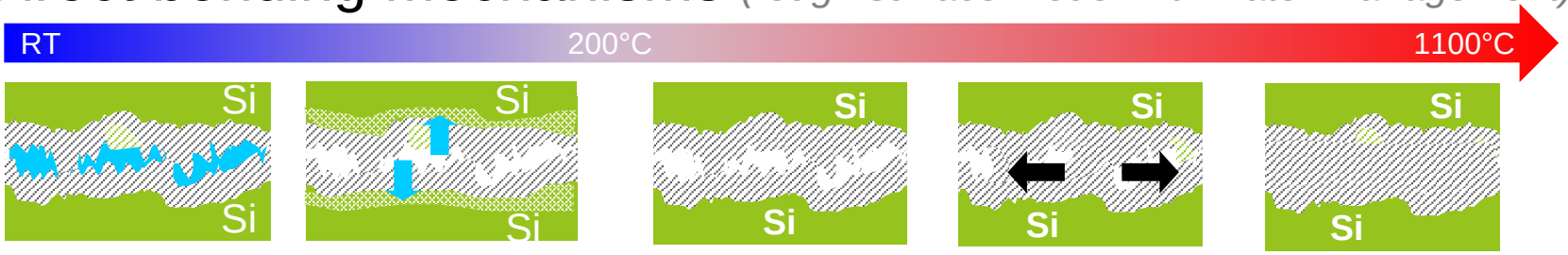




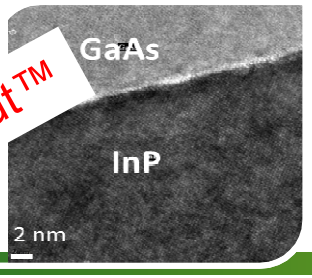


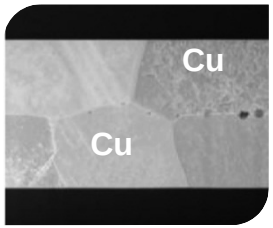


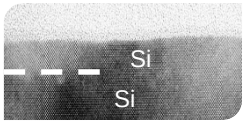
Direct bonding mechanisms *(rough surface model with water management)*

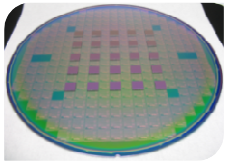


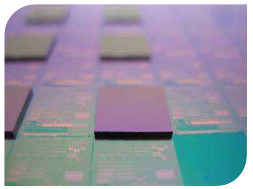
Some realizations

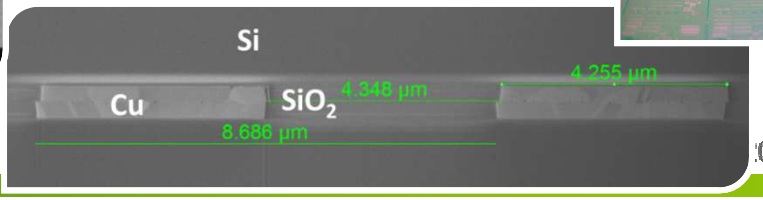








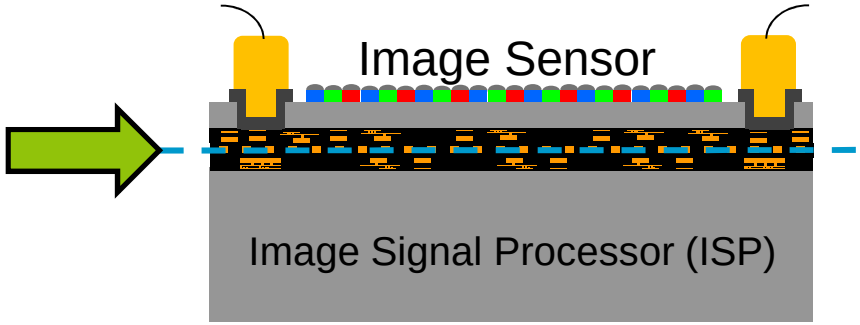




HYBRID DIRECT WAFER BONDING

New 3D imager sensor development with W2W hybrid bonding

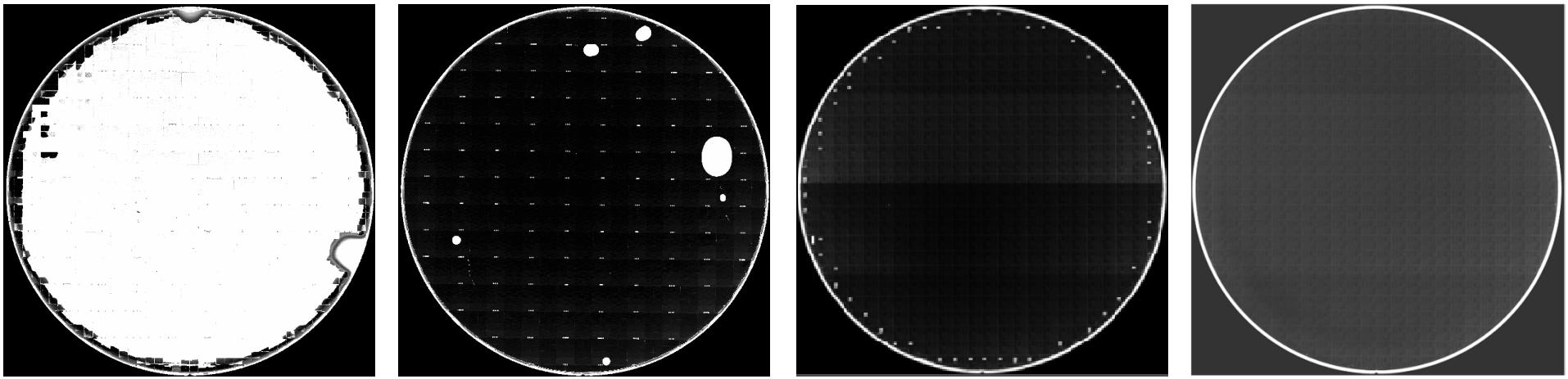
Hybrid bonding interface



STMicroelectronics & LETI collaboration

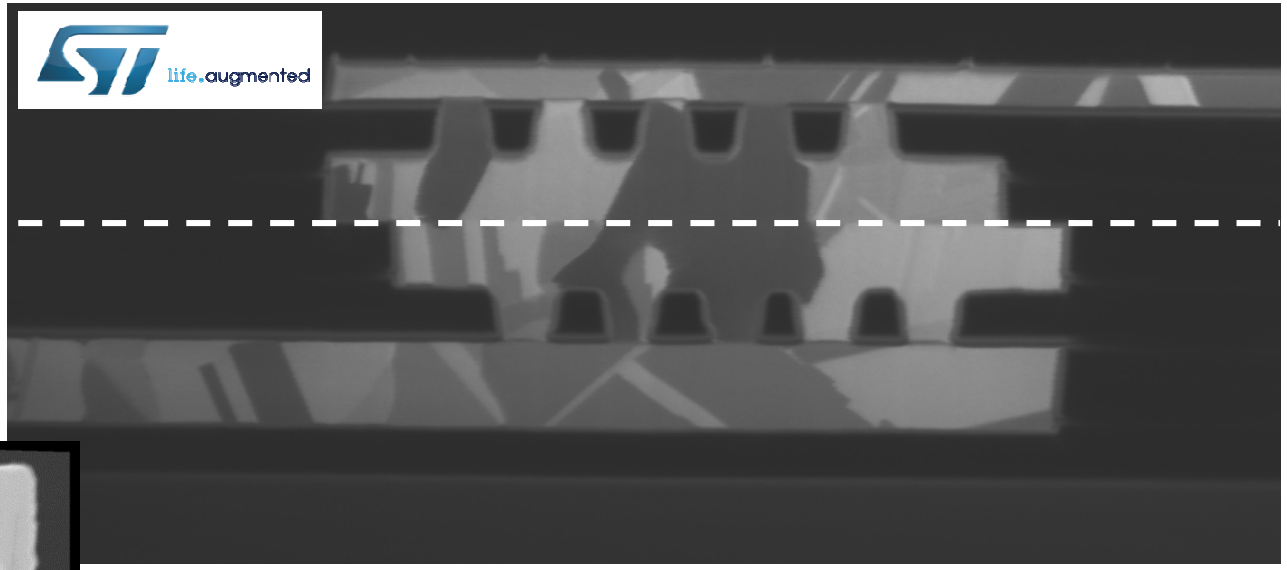
Direct hybrid bonding of BEOLs levels

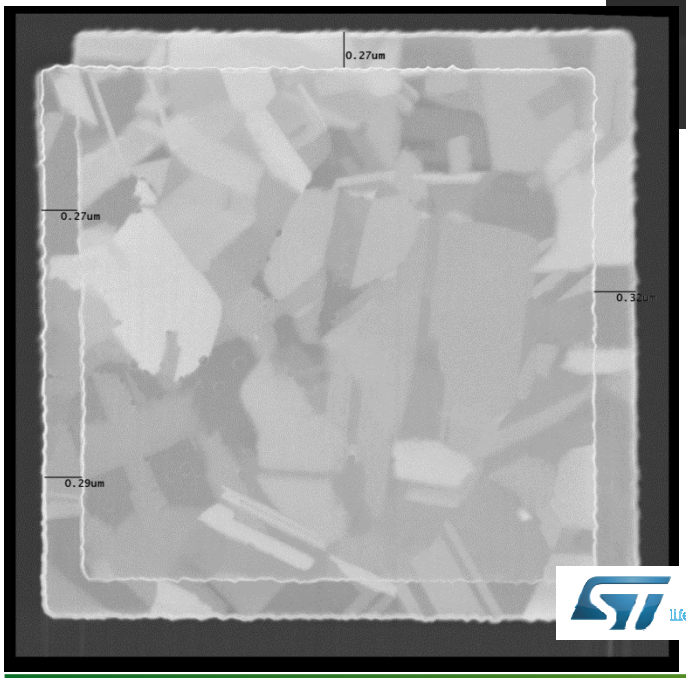
Surface preparation improvement

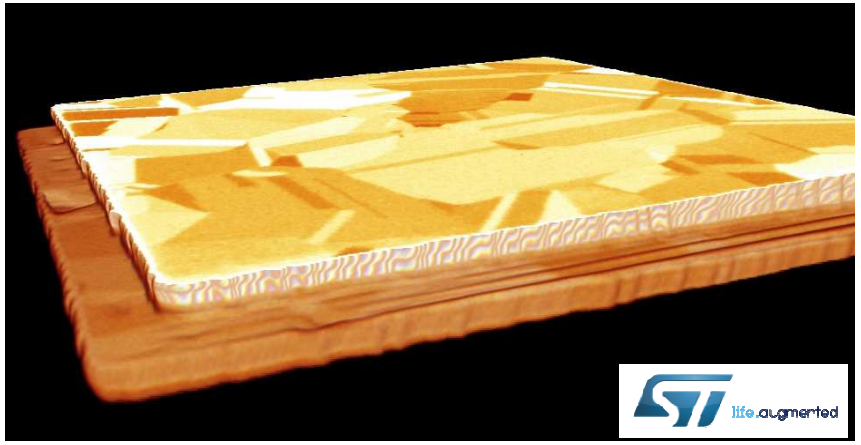


Hybrid bonding

Typical Cu/Cu bonding pad with Cu crystal growth during bonding interface disappearance.



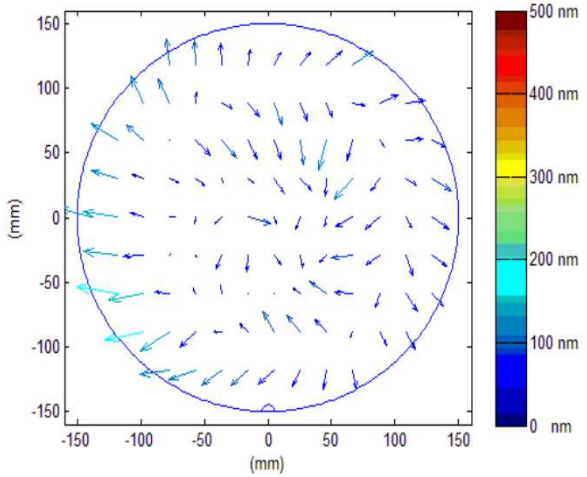




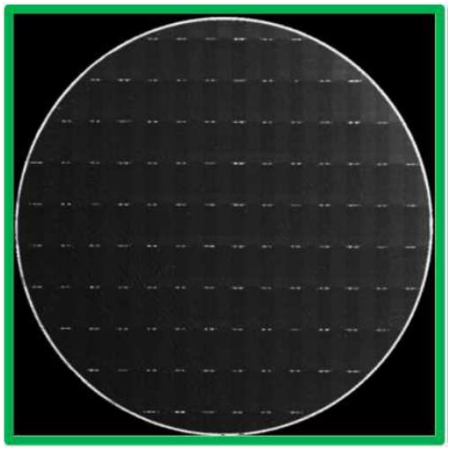
HYBRID DIRECT WAFER BONDING

Fine pitch

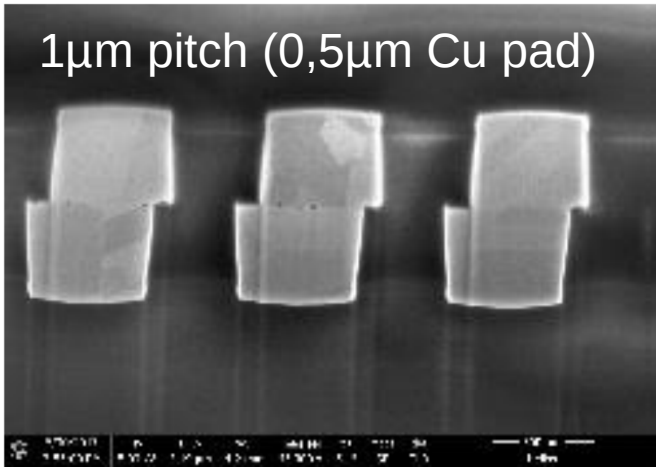
EVG Gemini



Global alignment : 10nm @ 3σ 195 nm



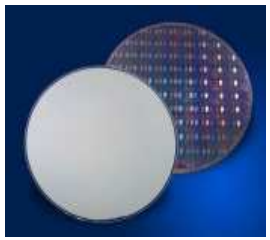
Post-bonding SAM characterization



DIRECT WAFER BONDING FOR MOORE LAW

SOI Substrates
Mobility booster (sSOI, GeOI, …)
Ultrathin Buried Oxide
Alternatives Buried Oxide (SiNx, C*, …)

soitec

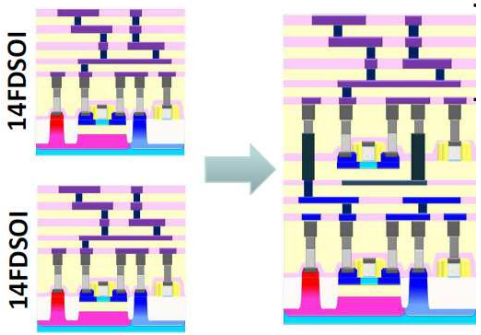


life.augmented

Alternative to Scaling

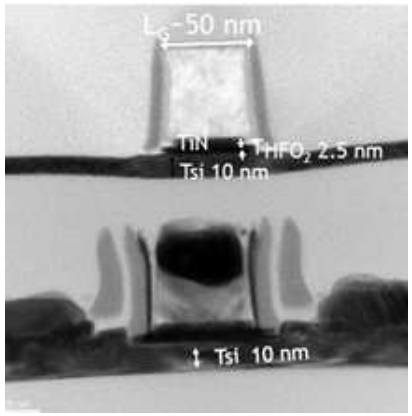
Monolithic 3D for further density scaling

Advanced substrates



IBM

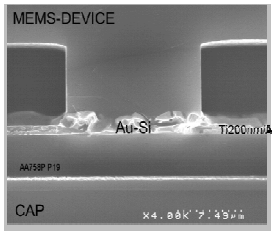
QUALCOMM®



life.augmented

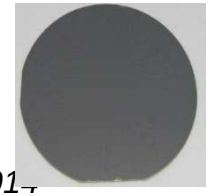
P. Batude, VLSI 2011

AND ENABLING MORE THAN MOORE…

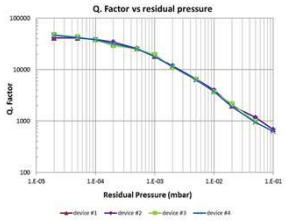


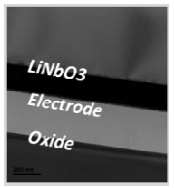
Hermetic Wafer Level Packaging

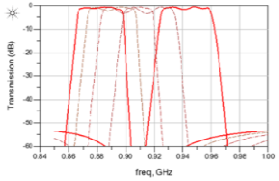
S. Nicolas et al, ECTC 2014

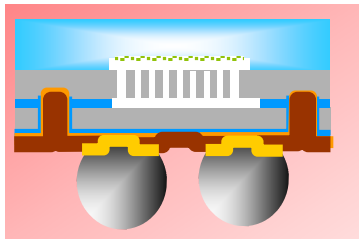


Soitec

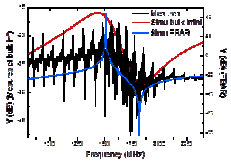








RF

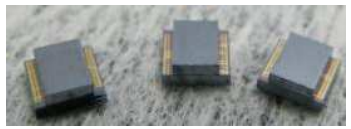


High performances RF Filters

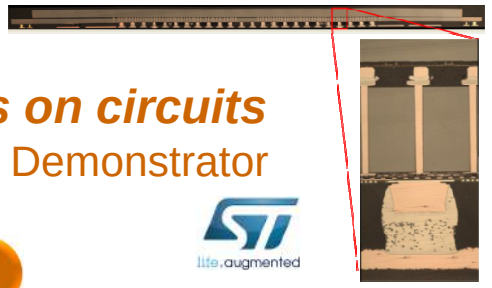
Piezoelectric thin film transfer

JS Moulet et al, IEDM 2008
B. Imbert, IFCS 2011
Undisclosed industrial partner

MEMS



Dutoit et al., VLSI Circuits 2013

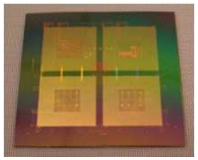


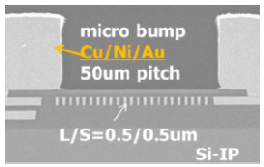
Circuits on circuits

Wide I/O Demonstrator

3D Applications

High density 3D Silicon Interposer

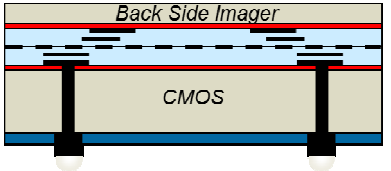


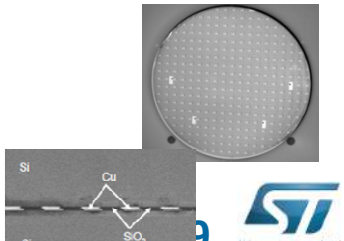


J. Charbonnier et al., ESTC 2012, ECTC 2013

SHINKO

3D stacked CMOS imager





R Taibi et al, IEDM 2011

CEA-LETI BONDING ECOSYSTEM

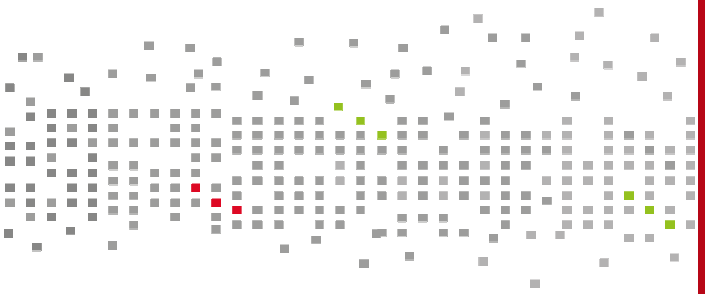
- Fundamental research through **academic collaborations**

- **R&D partnership** with
  - Soitec (20 years long collaboration)
  - EV Group (from 2013)
  - ST microlectronics

- Industrial **equipment suppliers** collaboration

- More than **60 patents** related to bonding tech. and app.
- **International recognition** with conference board
  - ECS (Wafer bond symposium), Wafer bond conference , EEE S3S conference …

Thank you !



Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 rue des Martyrs | 38054 Grenoble Cedex | France
www.leti-cea.com